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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/923,976	08/07/2001	Kirk Bresniker	10012569-1	2332

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EXAMINER	
MARTIN, NICHOLAS A	

ART UNIT	PAPER NUMBER
2154	

DATE MAILED: 01/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/923,976	BRESNIKER ET AL.	
	Examiner	Art Unit	
	Nicholas A. Martin	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/7/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/7/01, 3/19/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-20 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1, 6-9, 11, 14 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Crisan, Adrian (hereinafter Crisan), US 6,105,140.

3. As per claim 1, Crisan teaches a host processor card configured to be fitted into a server system (Col. 3, lines 34-39), the host processor card comprising:

a processor (Col. 3, lines 34-35);

a memory coupled to the processor for storing an operating system (Col. 2, lines 5-10; Col. 3, lines 46-48; Col. 12, lines 66-67; Col. 13, lines 1-3, lines 8-10);

a power control line for controlling the power state of the host processor card (Col. 3, lines 46-48; Col. 6, lines 16-20);

a graceful shutdown circuit coupled to the processor and the power control line, the processor configured to provide a graceful shutdown signal to the graceful shutdown circuit, the graceful shutdown circuit configured to allow a graceful shutdown of the host processor card when the power control line indicates that the host processor card is to be powered down if the processor has provided the graceful shutdown signal (Col. 6, lines 16-20, lines 60-67; Col. 7, lines 1-8).

4. As per claim 6, Crisan teaches the host processor of claim 1, wherein the processor includes a register for indicating when a graceful shutdown is to be performed, and wherein the operating system is configured to write a value to the register indicating whether a graceful shutdown is to be performed (Col. 2, lines 5-10; Col. 3, lines 46-48; Col. 8, lines 9-14; Col. 10, lines 35-40; Col. 12, lines 66-67; Col. 13, lines 1-3, lines 8-10).

5. As per claim 7, Crisan teaches the host processor of claim 6, wherein the operating system is configured to write a value to the register indicating that a graceful shutdown is to be performed when the operating system boots up to a point that an immediate shutdown should not be performed (Col. 4, lines 23-26; Col. 9, lines 25-34; Col. 10, lines 43-52; Col. 11, lines 9-15).

6. As per claim 8, Crisan teaches the host processor card of claim 1, wherein the graceful shutdown circuit further comprises a monitor circuit coupled to the power control line and coupled to the processor, the monitor circuit configured to provide an

indication of the status of the power control line to the processor (Col. 6, lines 18-23; Col. 7, lines 32-41).

7. As per claim 9, Crisan teaches the host processor of claim 1, wherein the graceful shutdown circuit further comprises a switch circuit coupled to the power control line and coupled to the processor, the switch circuit configured to override a power down signal on the power control line and thereby maintain power to the host processor card if the processor has provided the graceful signal to the graceful shutdown circuit (Col. 2, lines 39-46; Col. 6, lines 56-67; Col. 7, lines 1-8).

8. As per claim 11, Crisan teaches a graceful shutdown circuit for a host processor configured to be fitted into a server system, comprising:

a power control line for controlling the power state of the host processor card (Col. 3, lines 46-48; Col. 6, lines 16-20);

a monitor circuit for monitoring the state of the power control line, the monitor circuit including a first input configured to be coupled to a processor of the host processor card to indicate the state of the power control line (Col. 6, lines 18-23; Col. 7, lines 32-41, lines 54-58; Col. 8, lines 4-5);

a first input configured to be coupled to a processor of the host processor card, the first input indicating whether a graceful shutdown is to be performed (Col. 7, lines 54-58; Col. 8, lines 4-8); and

a switch circuit coupled to the first input and the power control line, the switch circuit configured to maintain power to the host processor card via the power control line

when the first input indicates that a graceful shutdown is to be performed (Col. 2, lines 39-46; Col. 6, lines 56-67; Col. 7, lines 1-8, lines 54-58; Col. 8, lines 4-5).

9. As per claim 14, Crisan teaches a method of gracefully shutting down a host processor card in a server system, the method comprising:

monitoring a power control line that controls the power state of the host processor card (Col. 6, lines 18-23; Col. 7, lines 32-41);

providing a graceful shutdown indication from an operating system of the host processor card to a processor of the host processor when an immediate shutdown of the host processor card should not be performed (Col. 9, lines 25-34; Col. 10, lines 43-51);

outputting a graceful shutdown signal from the processor when an immediate shutdown of the host processor card should not be performed (Col. 7, lines 54-58; Col. 8, lines 4-8);

overriding the power control line when the processor outputs the graceful shutdown signal, thereby maintaining power to the host processor card (Col. 2, lines 39-46); and

initiating a graceful shutdown of the operating system when the power control line provides a power down signal if the operating system has provided the graceful shutdown indication to the processor (Col. 10, lines 35-40).

10. Claim 19 does not teach or define any new limitations above claim 6 and therefore are rejected for similar reasons.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 2, 12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crisan, Adrian (hereinafter Crisan), US 6,105,140, in view of Byers et al. (hereinafter Byers), US 5,594,893.

12. As per claim 2, Crisan does not explicitly teach the host processor card of claim 1, wherein the graceful shutdown circuit is configured to allow an immediate shutdown of the host processor card when a received power control signal indicates that the host processor card is to be powered down if the processor has not provided the graceful shutdown signal.

13. Byers teaches a processor card wherein the graceful shutdown circuit is configured to allow an immediate shutdown of the host processor card when a received power control signal indicates that the host processor card is to be powered down if the processor has not provided the graceful shutdown signal (Col. 1, lines 35-46).

14. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Byers and Crisan because they both deal with shutdown procedures of processing units. Furthermore, the teaching of Byers to allow wherein the graceful shutdown circuit is configured to allow an immediate shutdown of the host processor card when a received power control signal indicates that the host

processor card is to be powered down if the processor has not provided the graceful shutdown signal would improve functionality of Crisan's system by allowing for operating system processes to close before power is removed.

15. Claims 12 and 15 do not teach or define any new limitations above claim 2 and therefore are rejected for similar reasons.

16. Claims 3-5 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crisan, Adrian (hereinafter Crisan), US 6,105,140, in view of Han et al. (hereinafter Han), US 5,989,043.

17. As per claim 3, Crisan teaches the host processor card of claim 1, wherein the power control is coupled to a switch to turn on the computer system (Col. 6, lines 56-60).

18. Crisan does not teach a switch that is configured to close when the host processor is inserted into the server system.

19. Han teaches a switch that is configured to close when the host processor is inserted into the server system (Col. 8, lines 19-26).

20. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Han and Crisan because they both deal with power switch on/off mechanisms. Furthermore, the teaching of Han to allow a switch that is configured to close when the host processor is inserted into the server system would improve functionality of Crisan's system by preventing a malfunction and damage of the system by accurately adjusting the on timing of the power switch.

21. As per claim 4, Crisan does not explicitly teach the host processor of claim 3, wherein the switch is configured to open when the host processor card is being

removed from the server system, causing the power control line to indicate that the host processor card is to be powered down.

22. Han teaches a plug-in processor card wherein a switch is configured to open when the host processor card is being removed from the server system, causing the power control line to indicate that the host processor card is to be powered down (Col. 2, lines 49-53; Col. 8, lines 27-34).

23. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Han and Crisan because they both deal with power switch on/off mechanisms. Furthermore, the teaching of Han to allow wherein a switch is configured to open when the host processor card is being removed from the server system, causing the power control line to indicate that the host processor card is to be powered down would improve functionality of Crisan's system by preventing a malfunction and damage of the system by accurately adjusting the off timing of the power switch.

24. As per claim 5, Crisan teaches the host processor of claim 3 or claim 4, wherein the power control line is coupled to a management controller that is configured to control the power state of the host processor card when the switch is closed (Col. 7, lines 4-8, lines 32-41, lines 63-67; Col. 8, lines 1-2).

25. Claim 16 does not teach or define any new limitations above claim 3 and therefore are rejected for similar reasons.

26. Claim 17 does not teach or define any new limitations above claim 4 and therefore are rejected for similar reasons.

27. Claim 18 does not teach or define any new limitations above claim 5 and therefore are rejected for similar reasons.

28. Claims 10, 13 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crisan, Adrian (hereinafter Crisan), US 6,105,140, in view of Ten Holter, Ronaldus Paulus Maria (hereinafter Ten Holter), US 6,351,083.

29. As per claim 10, Crisan does not explicitly teach the host processor card of claim 9, wherein the graceful shutdown circuit further comprises a manual emergency switch coupled to the switch circuit, the emergency switch configured to cause immediate shutdown of the host processor card.

30. Ten Holter teaches a processor card wherein the graceful shutdown circuit further comprises a manual emergency switch coupled to the switch circuit, the emergency switch configured to cause immediate shutdown of the host processor card (Col. 10, lines 61-67; Col. 11, lines 1-12).

31. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Ten Holter and Crisan because they both deal with the circuitry for power supply to electrical units. Furthermore, the teaching of Ten Holter to allow wherein the graceful shutdown circuit further comprises a manual emergency switch coupled to the switch circuit, the emergency switch configured to cause immediate shutdown of the host processor card would improve functionality of Crisan's system by allowing for immediate shutdown to increase safety of the circuit to protect against errors and emergency situations should they arise.

32. Claims 13 and 20 do not teach or define any new limitations above claim 10 and therefore are rejected for similar reasons.

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art with respect to the "System And Method For Graceful Shutdown Of Host Processor Cards In A Server System".

i. US 6,445,086 Houston, David H.

ii. US 5,546,590 Pierce, Michael E.

iii. US 5,758,171 Ramamurthy et al.

34. A shortened statutory period for reply to this Office action is set to expire in THREE MONTHS from the mailing date of this action.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nicholas A. Martin whose telephone number is (571) 272-3970. The examiner can normally be reached on Monday - Friday 8:30 a.m. - 5:30 p.m..

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A. Follansbee can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-3970.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

nam
January 3, 2005

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